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Abstract. The progress of the Jet Propulsion Laboratory in developing gallium arsenide junction field-effect transistors (GaAs JFETs) for application in infrared readout electronics operating below 10 Kelvin is discussed. Previously, discrete GaAs JFETs had been developed. By using a highly isotropic HF-based etchant, the typical input leakage current at 4 K had been reduced to less than 1 fA. These same devices had a low frequency noise of just under 1 $\mu V/Hz^{1/2}$ at 1 Hz at 4 K, while dissipating less than 1 μW of power. In this paper we report on the fabrication of small-scale integrated circuit multiplexers and amplifiers made using this GaAs JFET technology. Small 8x1 source-follower-per-detector multiplexers and differential pairs have been fabricated and are fully functional at 4 K. The input-referred noise and leakage current is consistent with that for the discrete devices. Differential amplifier pairs were also measured. A systematic study of the device size dependence of the noise has been started, but as yet is inconclusive.

1. INTRODUCTION

Imagers and spectrometers for very long wavelength infrared (VLWIR) astronomy typically use detector arrays cooled to deep cryogenic temperatures (below 10 K). Because conventional silicon readout electronics fail at these temperatures, designing readout electronics for VLWIR systems has been challenging. Many conventional systems use readout electronics based on a silicon JFET front end, held in a separate compartment at 55 to 80 K. This requires a separate wire for each detector to be run from the detector cold head to the warmer electronics compartment. The thermal isolation and noise suppression difficulties associated with this approach, as well as the limitations it imposes practical array size, has led to efforts to develop electronics that can operate below 10 K and be placed in immediate contact with the detector array. Several different approaches are being explored at different laboratories, including specialized cryogenic silicon CMOS [1], germanium devices, GaAs metal-gate field effect transistors (MESFETs) [2], and GaAs junction field effect transistors (JFETs) [3].

For the last several years, the NASA Jet Propulsion Laboratory has focussed on gallium arsenide junction field-effect transistors (GaAs JFETs) for deep cryogenic readout electronics. These JPL JFETs use molecular beam epitaxy (MBE) to form a grown junction, with wet chemical etch-back used to define the lateral device structure, and to isolate one transistor from another.

For deep cryogenic readout electronics applications, the important characteristics are the input leakage current (which must be kept comparable to the detector dark current), the power dissipation and the noise. Typically, the power dissipation must be at most a few microwatts per channel for VLWIR readout applications. Photoconductive and photovoltaic detectors, such as blocked impurity band detectors, usually require input leakage currents of a few hundred electrons per second or less and input-referred noise values of less than 1 $\mu V/Hz^{1/2}$ at 1 Hz. Bolometer readout applications usually are less restrictive on the leakage current but more demanding on noise, requiring input impedances hundreds of megaohms and input-referred noise voltages as low as 10 $nV/Hz^{1/2}$.

By using a highly isotropic HF-based etchant, JPL has been able to fabricate discrete GaAs JFETs with input leakage currents of less than 1 fA at 4 K, and with input-referred noise values of less than 1 $\mu V/Hz^{1/2}$ at 1 Hz when dissipating less than 1 μW of power. We have now progressed to small-scale integrated circuit readout amplifiers and multiplexers, based on this GaAs JFET technology. In the remainder of the paper, we discuss the basics of the JFET fabrication, the design of the multiplexers and amplifiers, and our plan for exploring and reducing the device noise.

2. THE GaAs JFET STRUCTURE

The JFET structure is shown in Figure 1. Starting on a semi-insulating GaAs substrate, MBE is used to grow an undoped buffer approximately 1 μm thick, followed by an n-type channel several thousand angstroms thick and capped with a p+ junction layer 500 Å thick. The channel is doped with silicon to a range of 10^{16} to 10^{17} cm^{-3}. The p+ junction layer is doped with beryllium to greater than $5x10^{18}$ cm^{-3}. After growth, the p-layer is etched back to expose the n-layer for source and drain contacts, and the transistor mesas are defined by etching down to the substrate.

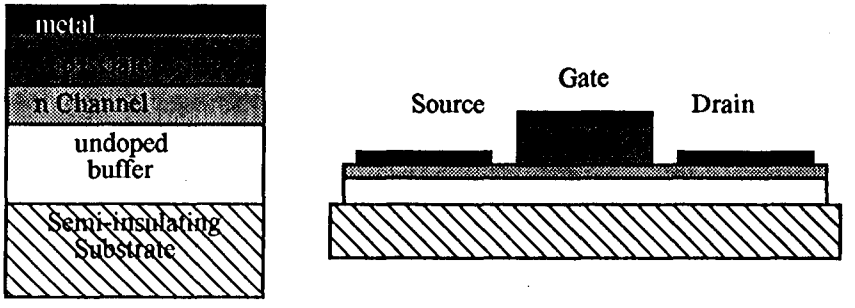

Figure 1: The structure of the GaAs JFET

Originally, the gate metallization was used as a mask for the gate wet chemical etching, and an ammonium hydroxide-base etch was used [4]. It was noticed however, that this resulted in faceting and other effects producing sharp edges that could concentrate electric fields and increase the leakage current through tunneling. Therefore in subsequent JFETs, a highly isotropic HF-based etchant was used with a photoresist mask to reduce sharp edges at the gate edge; the gate metal was deposited in a separate step. This reduced the input leakage to less than 1 fA. The noise reduced slightly as well, from just over 1 $\mu V/Hz^{1/2}$ to just under 1 $\mu V/Hz^{1/2}$ at 1 Hz [5].

3. MULTIPLEXER AND AMPLIFIER FABRICATION

Having demonstrated reasonable performance in discrete GaAs JFETs, we began the task of fabricating small-scale integrated circuit amplifiers. The basic device fabrication was the same as for the discrete JFETs, with the addition of a dielectric and an interconnect metallization. First, the individual JFETs were made using the gate etch, ohmic contact metallization, device isolation etch and gate metallization. Then, polyimide was spun on and cured. The contact openings were opened in the polyimide layer by reactive ion etching in an oxygen plasma, using a photoresist mask. Then, the contact metallization consisting of 20 nm of chromium under 200 nm of gold was deposited and patterned using lift-off. The pads for wire bonding were also formed from this metallization.

An 8x1 source-follower-per-detector multiplexer was fabricated by this method. An abbreviated schematic that shows the common circuitry and two of the eight cells of the array is shown in Figure 2. In actual operation, a VLWIR photodiode from an array would be connected to each of the input nodes.

Each cell contains three GaAs JFETs, one configured as a source-follower and the other two used as switches. The reset transistor in each cell connects the cell's input to the common V_{Reset} line. When the common ϕ_{Reset} line goes high, each of the reset transistors turns on, resetting the input of each cell. In actual operation this would also set the bias on the VLWIR photodiode connected to the input. When ϕ_{Reset} returns low, the JFET reset switches are opened, and the inputs of each cell are isolated. Ordinarily, the select lines for all cells are low, turning the JFET select switch off. To select a cell, the individual select line for that cell is brought high, turning the JFET select switch on and connecting the source of the source-follower JFET in that cell to the common output bus. The common load JFET at the bottom of the output bus is biased as a current source by V_{LN}. This constant current forces the source-follower to drive the output bus to a voltage equal to the voltage on the input node for that cell, with a fixed voltage offset.

A simple differential pair was also included on the mask set with the multiplexer. It consists of a pair of JFETs with separate gate and drain contacts. The sources of the JFETs are joined and connected to a common current load JFET. This differential pair is also shown in Figure 2.

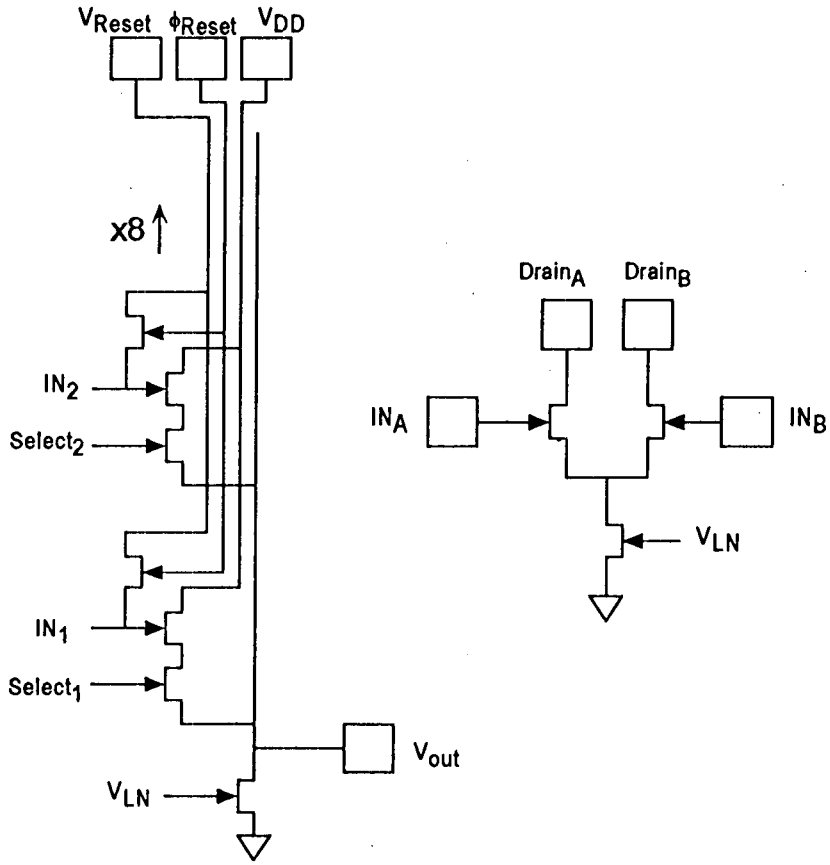

Figure 2: The schematics of small-scale integrated circuits made from GaAs JFETs. Shown on the left is part of an 8×1 multiplexer. Two of the eight pixels are shown, along with the common current-source load transistor and the column lines and pads. Shown on the right is a simple differential pair including a common current load transistor.

4. MULTIPLEXER NOISE AT 4 K

The multiplexer shown in Figure 2 was tested by using an external current source connected to the output, rather than using the internal current source. The multiplexer was biased at a current of 50 μA. This relatively large current was used so that the capacitance of the several meters of output cabling would not limit the frequency response of the circuit, which would distort the output noise signal. The input was biased by pulsing ϕ_{Reset} high, then isolated by returning ϕ_{Reset} low. The output voltage noise with the input

isolated was recorded using an HP3561 dynamic signal analyzer. The resulting noise performance is shown in Figure 3.

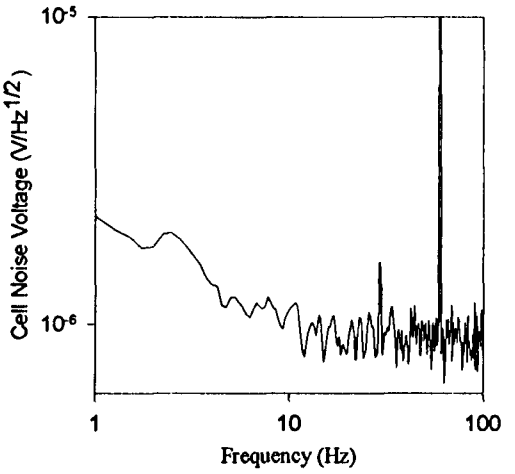

Figure 3: The output noise voltage from one cell of the 8x1 multiplexer at 4 K with the input floating and isolated. The source-follower was biased with an external current source of 50 μA, and the measured source-follower gain was 0.88. The noise spike at 60 Hz is line frequency pickup.

5. SYSTEMATIC NOISE STUDIES ON DISCRETE DEVICES

In order to better characterize the noise, we have fabricated chips consisting of a set of discrete JFETs ranging in size from 20 μm × 10 μm to 500 μm × 500 μm, fabricated using the isotropic etch technology. A table listing the size of these JFETs is shown in Table 1. We have also fabricated chips where there are multiple versions of JFETs of the same size. We are now measuring the noise performance of these discrete JFETs at 4 K in order to determine whether there is a systematic dependence of the noise on the device perimeter or area. This study is not yet complete, but preliminary results indicate that the random device to device variation, even among devices of the same size, is at this time larger than any systematic size dependence of the noise.

Table 1: The sizes of the GaAs JFETs on a single chip, used to study the size dependence of the noise and other parameters. JFETs A, B, and C are ring structure FETs: the width is the circumference of the ring gate and the length is the thickness of the ring. All of the other JFETs are rectangular.

Label	Width (μm)	Length (μm)
A	1250	50
B	625	50
C	315	50
D	10	500
E	100	400
F	90	200
G	45	200
H	45	100
I	25	200
J	25	100
K	25	50

Label	Width (μm)	Length (μm)
L	500	10
M	100	10
N	50	10
O	20	10
P	20	20
Q	100	20
R	500	500
S	20	50
T	50	500
U	50	100
V	50	50

6. SUMMARY

In summary, we had previously demonstrated GaAs JFETs functional at 4 K, and by employing an isotropic HF-based etchant we had reduced the input leakage current to less than 1 fA. At this point, the GaAs JFET technology was mature enough for some VLWIR detector readout applications.

Using this GaAs JFET technology, we have fabricated and tested prototype readout circuits at 4 K. The output noise from a cell of an 8x1 multiplexer at 4 K with a 50 μA bias and with the input isolated was just over 1 $\mu V/Hz^{1/2}$ at 1 Hz. This noise is low enough for the readout of some photoconductive and photovoltaic detectors, but at least an order of magnitude too high for bolometer readouts.

We are now focussing on reducing this noise voltage. A set of JFETs of widely different sizes has been fabricated to help characterize the noise, but so far any systematic size dependence is masked by the larger device to device variation.

Acknowledgments

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References

[1] Young E.T., "Progress on readout electronics for far-infrared arrays", Infrared Readout Electronics II, Orlando, Florida, USA 7-8 April 1994, E.R. Fossum Ed. (Proc. of the SPIE, **Volume 2226**, Bellingham, Washington, USA, 1994) pp. 21-28.

[2] Camin D.V. and Pessina G., "Cryogenic ASICs in GaAs for Applications with Particle Detectors," WOLTE 2, Leuven, Belgium 26-28 June 1996, C. Claeys and E. Simoen Eds. (Jour. de Physique IV, **Volume 6**, Les Éditions de Physique, Les Ulis, 1996) pp. C3 225-230.

[3] Kirschman R.K. and Lipa J.A., "Further Evaluation of GaAs FETs for Cryogenic Readout," Infrared Detectors and Instrumentation, Orlando, Florida, USA 14-16 April 1993, A. Fowler Ed. (Proc. of the SPIE, **Volume 1946**, 1993) pp. 350-364.

[4] Cunningham T.J. and Fossum E.R., "GaAs JFETs intended for deep cryogenic VLWIR readout electronics," WOLTE 1, Grenoble, France 29 June - 1 July, 1994, G. Ghibaudo and F. Balestra Eds. (Jour. de Physique IV, **Volume 4**, Les Éditions de Physique, Les Ulis, 1996) pp. C6 147-152.

[5] Cunningham T.J., "Improvements in GaAs JFETs for deep Cryogenic Operation," WOLTE 2, Leuven, Belgium 26-28 June 1996, C. Claeys and E. Simoen Eds. (Jour. de Physique IV, **Volume 6**, Les Éditions de Physique, Les Ulis, 1996) pp. C3 231-236.